Assembly and integration of semiconductor nanowires for functional nanosystems*

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Abstract: Central to the bottom-up paradigm of nanoscience, which could lead to entirely new and highly integrated functional nanosystems, is the development of effective assembly methods that enable hierarchical organization of nanoscale building blocks over large areas. Semiconductor nanowires (NWs) represent one of the most powerful and versatile classes of synthetically tunable nanoscale building blocks for studies of the fundamental physical properties of nanostructures and the assembly of a wide range of functional nanoscale systems. In this article, we review several key advances in the recent development of general assembly approaches for organizing semiconductor NW building blocks into designed architectures, and the further integration of ordered structures to construct functional NW device arrays. We first introduce a series of rational assembly strategies to organize NWs into hierarchically ordered structures, with a focus on the blown bubble film (BBF) technique and chemically driven assembly. Next, we discuss significant advances in building integrated nanoelectronic systems based on the reproducible assembly of scalable NW crossbar arrays, such as high-density memory arrays and logic structures. Lastly, we describe unique applications of assembled NW device arrays for studying functional nanoelectronic–biological interfaces by building well-defined NW-cell/tissue hybrid junctions, including the highly integrated NW–neuron interface and the multiplexed, flexible NW–heart tissue interface.

Keywords: assembly; integration; nanobiotechnology; nanoelectronics; nanowires.

INTRODUCTION

Nanoscience and nanotechnology represent an exciting and rapidly growing interdisciplinary research area that has begun to revolutionize a broad range of research fields, including chemistry, physics, materials science, engineering, energy, and the life sciences [1–8]. The remarkable development in nanoscale science and technology over the past decade has led to the building of virtually any kind of powerful device or functional system, ranging from nanoscale transitors [9–13], p-n diodes [14–16], light-emitting diodes (LEDs) [17], nanolasers [18], nanoresonators [19,20], to ultrasensitive chemical/biological sensors [21–23], high-efficiency and promising energy devices [24–28], and highly integrated nanocomputing systems [16,29–33]. The bottom-up paradigm for nanoscience and nanotechnology has the great potential to go far beyond the limits and functionality of the traditional "top-down" approach, leading to entirely new device concepts and novel functional systems. Central to efforts to develop the

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bottom-up approach for nanotechnology are several key areas shown in Fig. 1 [3]. The first and essential area is the synthesis of nanoscale building blocks [e.g., quantum dots, nanotubes, nanowires (NWs), etc.] with precisely controlled and tunable chemical composition, structure, size, morphology, and correspondingly defined electronic, optical/magnetic properties [34–38]. Secondly, it is critical to study comprehensively and understand the fundamental properties of these nanoscale structures, and further explore their physical limits as functional devices. Third and central to the bottom-up concept, hierarchical assembly strategies must be developed that eventually enable the organization of these building blocks into highly integrated nanosystems with predictable and versatile functions. Such techniques have recently been intensively explored, and a number of assembly methods have been demonstrated to achieve ordered arrays of nanostructures [39–48]. Last, the advantages and applications of these bottom-up assemblies need to be explored, characterized, and fully developed.
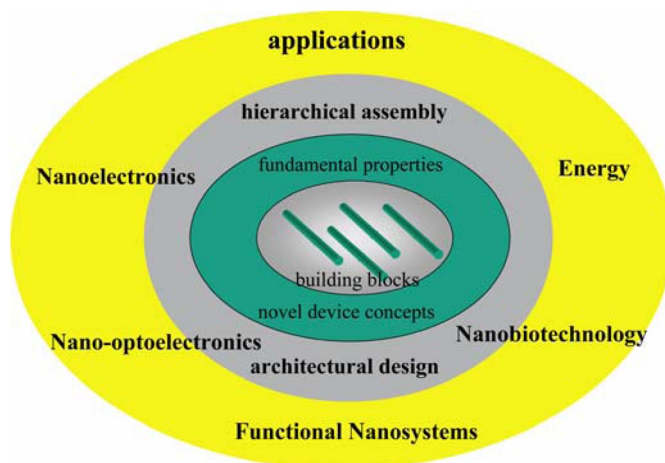

Fig. 1 Overview of the bottom-up paradigm for nanoscience and nanotechnology. Adapted from [3].

In this review, we will focus on one promising class of 1D nanostructures: semiconductor NWs. These nanostructures have been demonstrated to be one of the best-defined and highly diverse classes of nanoscale building blocks for realization of complex nanosystems in electronics, optoelectronics, and biotechnology. First, NWs can be rationally synthesized in single-crystalline form with key system parameters including NW diameter, length, doping, growth direction, and chemical composition, controlled during growth. Such synthetic controllability enables a wide range of nanoscale devices to be achieved and studied in a rational manner. Second, NWs can be grown in large quantities, subsequently assembled at large scale to form ordered arrays, and finally integrated as high-density nanodevices. Last, semiconductor NWs can possess unique surface functionality, either intrinsic or chemically modified, enabling the NWs to be fully compatible with and actively interact with chemical and biological systems.

Here we review a series of key advances in areas of both developing novel assembly approaches for organizing semiconductor NW building blocks into designed architectures and integrating ordered structures to construct functional NW-based nanosystems. We first introduce several rational assembly strategies recently developed for controlled organization of NWs into hierarchically ordered structures. Next, we discuss significant progress in building integrated nanoelectronic systems based on assembled NW crossbar arrays for high-density memory arrays and logic structures. Last, we describe unique applications of assembled NW device arrays for creating and studying functional nanoelectronic–biological interfaces.

HIERARCHICAL ASSEMBLY STRATEGIES

The development and implementation of efficient and scalable strategies for assembly and controlled organization of 1D NWs and nanotubes (NTs) are critical to both fundamental studies and the realization of many proposed applications based on these nanoscale building blocks. First, effective methods are needed to assemble NWs into highly integrated arrays with controlled orientation, alignment density, and spatial position. Second, these assembly approaches should be able to hierarchically organize NWs on multiple length scales and to make well-defined interconnections between nano-, micro-, and macroscopic worlds. To realize rational organization and integration, much effort has been devoted to developing complementary strategies for hierarchical NW assembly on functional surfaces [39–48]. In the following section, we will describe a series of assembly strategies for NW structures with emphasis on the most recently developed blown bubble film (BBF) technique and chemically driven assembly approach.

Overview of NW assembly methods

To construct NW-based functional nanosystems and realize their promising applications, considerable effort has been placed on developing methods of assembly of NWs [39–48]. For example, electrical field (E-field) can be applied to attract and align semiconductor NWs due to their highly anisotropic structures and polarizability [9,45]. Various configurations of assembled NW structures, including both parallel and crossed arrays, can be achieved through E-field-directed processes (Fig. 2a). Another example is microfluidic flow, which can be used to align NW structures by passing a suspension of NWs through microfluidic channels. The NWs are aligned along the flow direction driven by the shear force, and the density of assembled NWs is controlled by the concentration of NWs in the suspension and flow time. Complex geometries such as crossed NW arrays can be formed through a layer-by-layer process (Fig. 2b) [39]. Optical traps can also be generated to manipulate NW objects in a fluid environment [46,47]. These methods demonstrate some degree of control in assembling NWs, but they are still limited by the need for lithographically defined electrodes and microfluidic channels, etc.

The Langmuir–Blodgett (LB) technique, in which an ordered monolayer is formed on water and transferred to a substrate, represents a powerful approach to achieve NW assembly on larger scales with precise NW spacing down to the nanometer level. In the LB method of NW assembly, surfactant-wrapped NWs are slowly compressed on an aqueous subphase to yield uniaxially aligned NWs (Fig. 2c) [40,41]. Parallel and crossed NW structures with high density have been assembled by single and sequential transfer steps over centimeter length scales; moreover, functional devices based on such NW LB films have been fabricated [49], although it is unclear whether the centimeter-square arrays of NWs can be scaled further to larger areas with high efficiency and transferred to non-rigid surfaces, such as flexible plastics.

Another assembly strategy developed recently is a contact transfer technique that utilizes shear force generated by mechanically sliding two solid surfaces with respect to each other, where one surface is the NW growth substrate and the other is the device substrate [44,50]. The mechanically generated force enables the assembly of vertically grown NWs from growth substrate into oriented NW arrays on the target device substrate with an orientation parallel to the direction of sliding, as illustrated in Fig. 2d. The target device substrate is pre-patterned by lithography to facilitate the transfer of NWs to form well-aligned arrays on pre-defined regions after the removal of resist materials. A crossed NW configuration can be readily achieved by sequentially assembling the NWs in two orthogonal directions. This process provides a general platform for assembly of a variety of NW materials, and the process simplicity and low temperature requirement of the method make it suitable for many promising applications. For example, this method has been used to demonstrate the building of high-performance 3D integrated circuitry with different functionalities in distinct layers [44,51]. To elaborate a 3D structure,
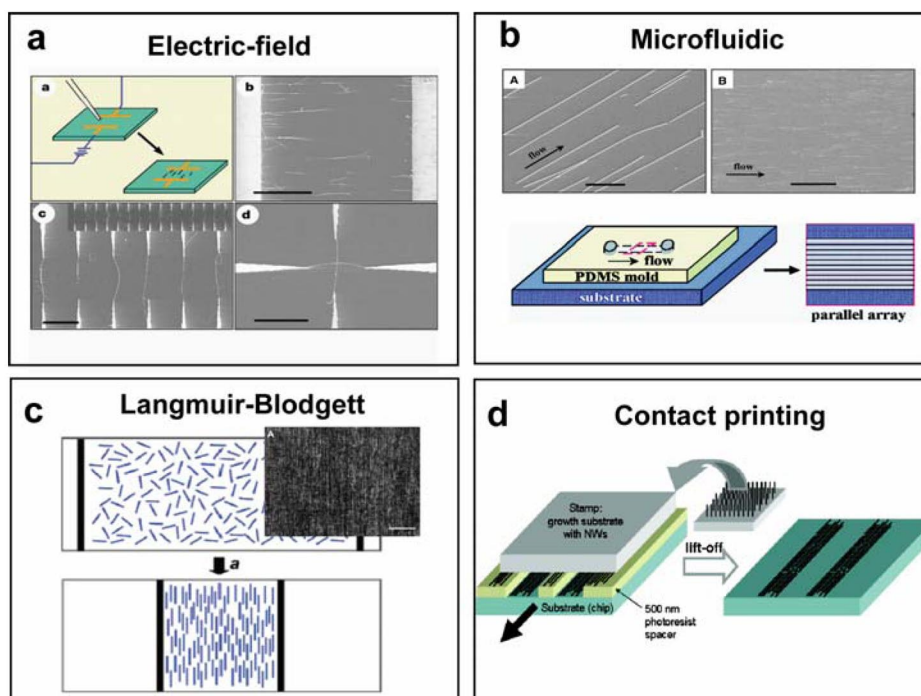
Fig. 2 Overview of assembly methods developed recently for NW systems, including electric/magnetic field-assisted (adapted from [9]), microfluidic flow (adapted from [39]), LB technique (adapted from [40]), and recently developed contact printing approach (adapted from [44]).

the NW printing and device fabrication steps are iterated multiple times, along with the introduction of an intervening insulating buffer layer for vertically stacked electronic layers.

Additional assembly methods for 1D nanostructures have used magnetic fields to direct the assembly of magnetic wires [48], dielectrophoresis [52], molecular forces such as van de Waals interactions and hydrogen bonding [53], electrostatic interactions [54], and also DNA has been used to direct and/or assist the assembly/alignment of NTs and NWs [55]. However, the question still remains whether these processes will enable the assembly to be scaled from the present centimeter regime to large wafers, which represent a scale important to many proposed electronic and photonic applications, and even areas as large as the meter scale, which open up unique opportunities in large-area displays and photovoltaics.

BBF technique for large-area, controlled-density, aligned NWs and NTs

Rationally organized 1D nanostructures with well-controlled location, orientation, and spacing across multiple length scales could enable next-generation high-performance electronic, optoelectronic, and electromechanical systems. Although several techniques have been developed for assembling nanoscale structures in the past few years [39–41,44–50,52–55], these methods have limitations with respect to scaling up to larger areas, potentially meter-scale, for many practical applications and/or efficient processing and transferring of the assembled structures to non-rigid surfaces or unconventional substrates. It is still imperative to promote the large-scale assembly of well-ordered nanostructures with controlled orientation and density into hierarchical functional systems on a wide range of substrates.

To this end, a general and scalable assembly method has been recently developed for uniformly aligned and controlled-density NW and NT films by controlling bubble expansion of homogeneous
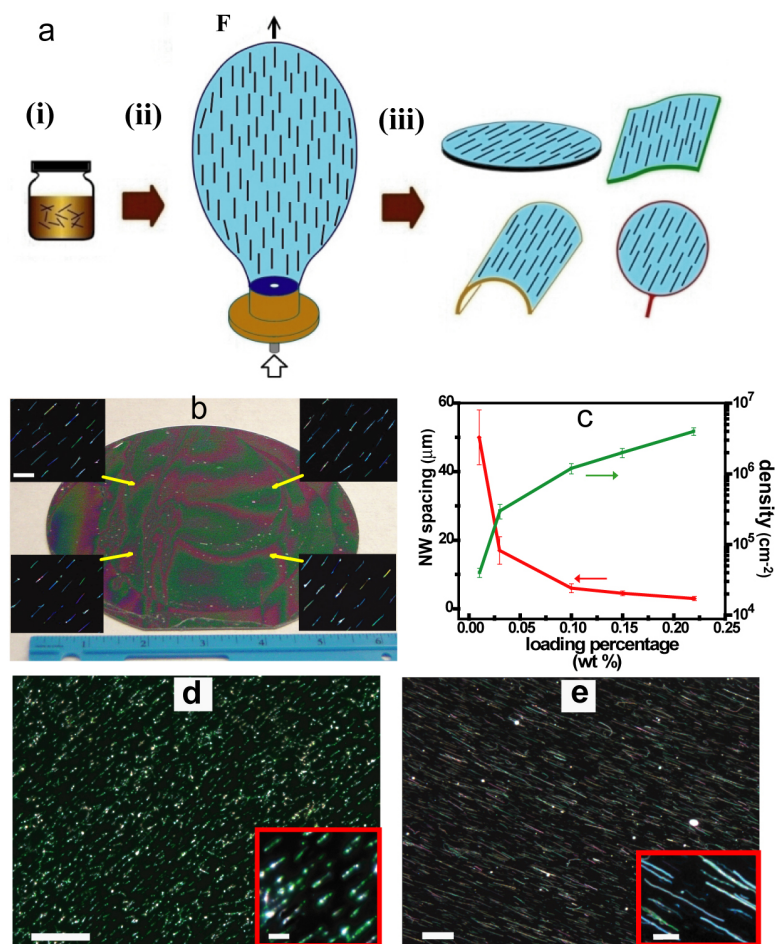
Fig. 3 Schematic illustration of BBF process and different materials-based BBFs. (a) (i) Stable polymer suspension containing nanomaterials, (ii) controlled bubble expansion over a circular die, (iii) films transferred to different surfaces: crystalline wafers, plastics, curved surfaces, and open frames; (b) optical image showing uniformly transferred bubble film on 6-in wafer with well-aligned Si NWs, scale bar: 10 µm; (c) density vs. concentration curve, indicating the density can be controlled by loading a percentage of nanomaterials; (d) optical image showing highly ordered single-walled carbon nanotubes (SWCNTs) in the bubble film, scale bar: 10 µm, (inset, 2 µm); (e) optical image showing multi-walled CNTs well aligned in the bubble film, scale bar: 25 µm (inset, 5 µm). Adapted from [42].

polymer suspensions containing these nanomaterials [42,43]. The BBF approach involves three steps, shown in Fig. 3a. First, a homogeneous, stable, and controlled concentration polymer suspension of different nanomaterials is prepared by chemically functionalizing the surface of the nanomaterials used. Secondly, bubble expansion of the polymer suspension is controlled using a circular die to form a bubble at controlled pressure P, and expansion rate via motor-directed force F. Finally, the BBFs are uniformly and conformally transferred to different substrate structures.

The BBF approach for assembling nanostructures has several distinct advantages compared with other assembly methods developed previously. First, this approach is general and can be used for organizing a broad range of nanomaterials with high-degree orientational alignment and controlled density, including a variety of semiconductor NWs, multi-walled NTs (MWNTs), and single-walled (SWNTs) (Figs. 3b,d,e), and in principle could be applicable to organize many other nanostructures such as

nanobelts and nanoparticles. Second, the nanomaterial-incorporated BBFs can be transferred to virtually any substrates or surfaces over large areas, including crystalline wafers, flexible plastics, and highly curved surfaces, to make large-scale functional nanodevice arrays (Figs. 4a–d). Third, this approach is highly scalable with potential to achieve meter-scale dimensions given the potential of blown film extrusion technique well established in the plastics industry. This represents one of the most critical advances in large-scale assembly of nanomaterials necessary for ultimately realizing applications and efficient processing of these nanomaterials in electronics and optoelectronics.
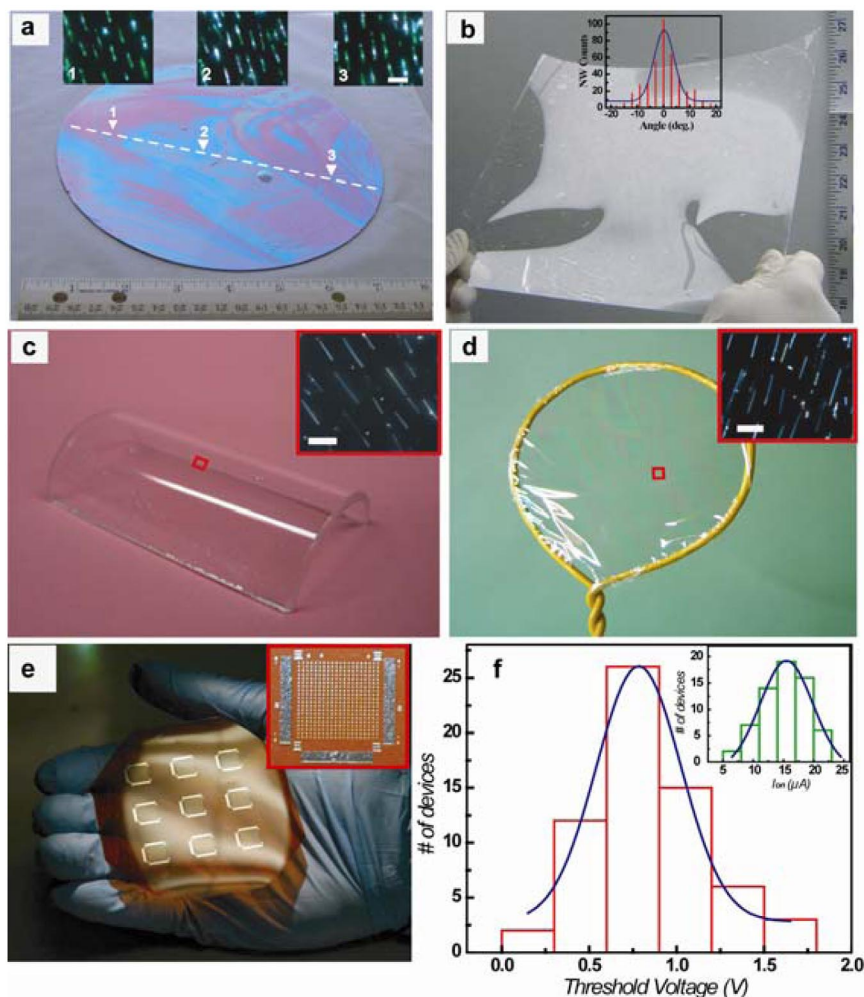

Fig. 4 BBF transfer and device array fabrication. (a) Uniformly aligned SWNT-BBF coated on 8-in Si wafer, scale bar: 2 μm (inset); (b) Si NW-BBF coated on 9 × 12 in plastic sheet; (c) bubble film transferred onto highly curved half-cylinder; (d) freestanding bubble film suspended across open frame; (e) flexible plastic substrate containing large arrays of NW transistor arrays; (f) histograms of on-current and threshold voltage show the excellent uniformity of device characteristics, indicating the reproducibility and reliability of this method for making large-scale devices. Adapted from [42].

Large-scale nanomaterial BBFs with distinct nanomaterial properties, including metallic conduction, semiconductor properties, and optical emission, can serve as a powerful platform for manufacturing electrically and/or optically active films for many applications. For example, we have successfully fabricated large-scale arrays of Si NW-based transistors on flexible, transparent polyimide substrate (Figs. 4e,f). Histograms of on-current and threshold voltage determined from analysis of a large number of fabricated devices confirm the excellent uniformity of device characteristics and reproducibility and reliability of this method for making large-scale devices.

Recently, this approach has been extended to different polymer systems (photoresist and water-soluble polymers) to advance reliable and reproducible device fabrication of as-assembled nanomaterials, making them unique structures for studying interfaces with biological systems [56]. The BBF approach has a huge potential for opening up a broad range of nanotechnology applications and new scientific directions. For example, nanostructure BBFs could be fabricated as reinforced nanocomposite films/coatings with visible/infrared absorption and fluorescence, thus enabling a new generation of super-smart materials that have novel function (as composites) and interactive reporting via optical signaling. NW/NT-BBFs are also yielding the largest flexible nanoelectronic systems to date—a factor critical for commercialization—including integrated high-performance field-effect transistors (FETs) and chemical/biological sensors for environmental and medical applications [21–23]; ultra-large-area, high-density flat panel displays; and large-scale solar panels [24–28]. Moreover, by layering multiple nanostructure BBFs or folding/scrolling nanomaterial BBFs, more complex 3D structures such as cross-bars and hierarchically arranged nanoscale building blocks can be fabricated to enable completely new types of electronic/photonic systems in the near future.

Chemically driven assembly of integrated NW system

The BBF technique that represents a novel and powerful assembly strategy for ultra-large-scale assembly of 1D nanostructures has certain limitations in terms of a lack of control over specificity and selectivity between NWs and target substrates, i.e., selective patterning/positioning of different types of NWs onto specific locations on functional substrates to build increasingly complex NW architectures [42,43]. To achieve a greater flexibility in rational assembly of 1D nanostructures into integrated nanosystems, we further developed a solution-based chemical approach that exploits complementary and selective chemical interactions to drive the rational organization of NWs into well-ordered arrays [57].

The underlying idea in this approach is to organize different types of functional semiconductor NWs by design of complementary chemical interactions between the surfaces of NWs and substrates. To highlight the versatility of chemical interactions, we demonstrate the complementary design of both covalent and noncovalent interactions on the surfaces of NWs and corresponding substrates, including covalent interactions based on thiol binding, electrostatic chemical interactions, and hydrogen-bond interactions (Fig. 5).
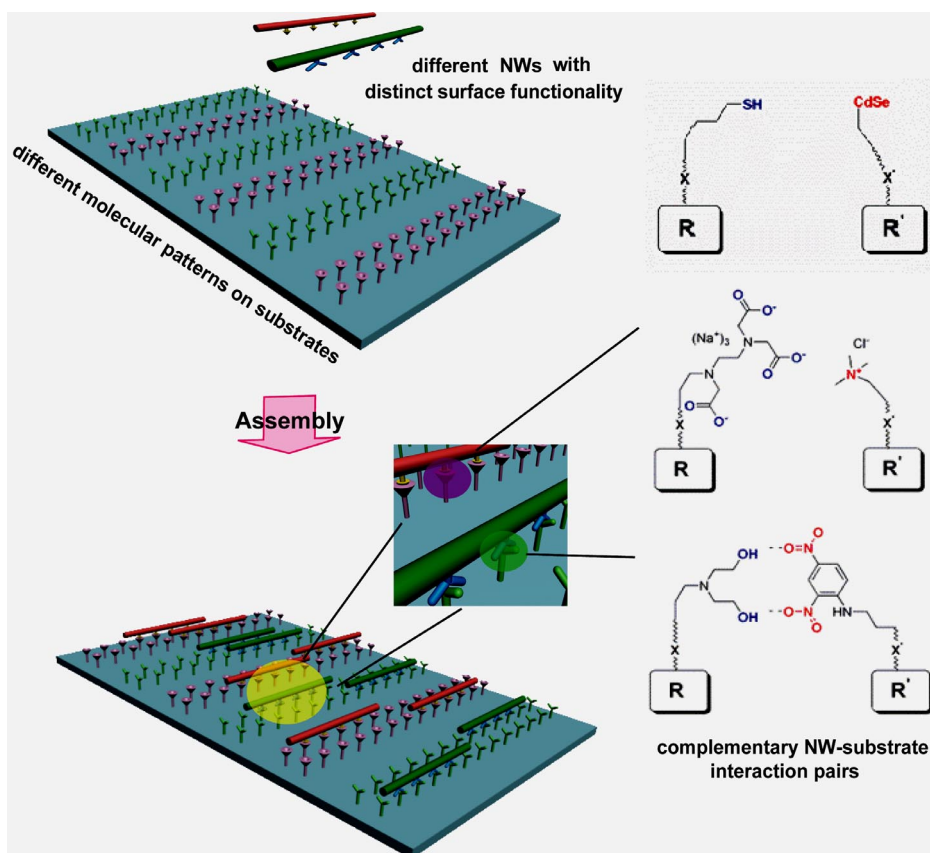
Fig. 5 Schematic illustration of chemically directed assembly of NW systems. Rationally chosen molecules are patterned on a Si/SiO$_2$ substrate and are ready for specific assembly of NWs with complementary surface functionality. The complementary NW–substrate interaction pairs used in the "bottom-up" NW assembly include thiol-based covalent interactions, electrostatic chemical interactions, and hydrogen-bond interactions.

The generality of this approach through the assembly of a chemically distinct NW system is also explored from single-element Si NWs to luminescent compound semiconductor NWs (groups II–VI). Specifically, for demonstration of covalent-bond-driven assembly, we choose the group II–VI compound semiconductor cadmium selenide (CdSe) NW as an example where the intrinsic surface has strong affinity to molecular patterns of thiol groups when modified on target substrate (SiO$_2$/Si). Alternatively, we functionalized Si NW surfaces to be complementary to molecular groups on a Si/SiO$_2$ substrate surface for demonstration of electrostatic and hydrogen-bond-directed NW assembly. Figures 6a–d clearly demonstrate that Si or CdSe NWs can be selectively assembled and aligned on complementarily modified regions on dielectric Si/SiO$_2$ substrates.

Moreover, we have shown that the design of different chemical patterns on substrates can be exploited to achieve selective and direct positioning of different types of NWs at well-defined locations on the same substrate. Figures 6e,f demonstrate that integrated arrays of Si NWs and compounds II–VI photoluminescent NWs were assembled onto the same functional substrate. Significantly, these results enable the building of complex nanostructures consisting of distinct NW elements necessary for realizing functional nanosystems. Given various surface functionalities achievable either with intrinsic surface properties or modification chemistry within NW systems, this chemically driven assembly
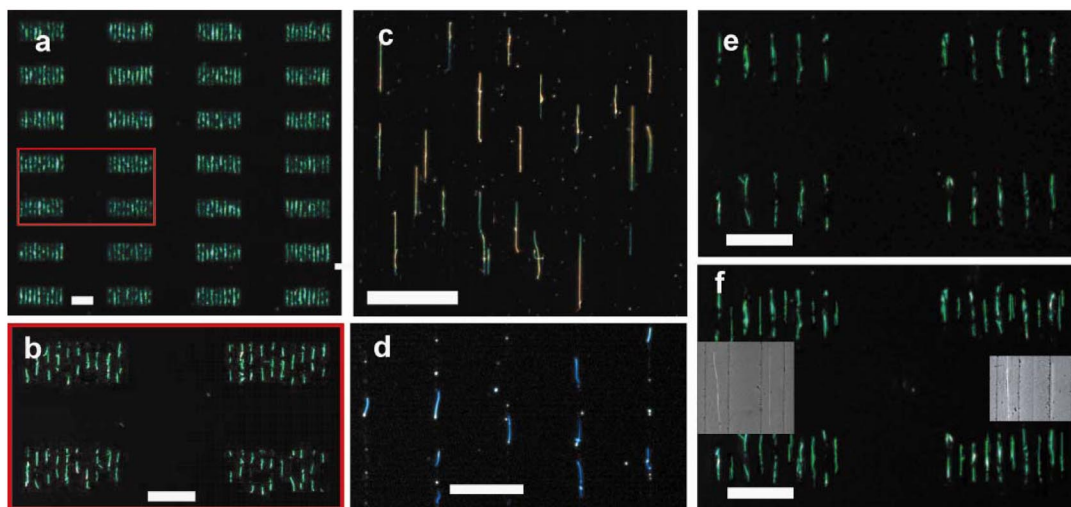
Fig. 6 Selective chemical interactions direct the assembly of NWs. (a,b) Dark field (DF) optical images of CdSe NWs that were selectively assembled and aligned on thiol-modified regions; (c) optical image of $-NH_3^+$-modified Si NWs well aligned on the $-COO^-$ molecular patterns; (d) optical image showing that $-NO_2$-modified Si NWs were self-assembled on $-OH$-modified regions following molecular line patterns; (e,f) optical images showing that arrays of CdSe NWs were first assembled onto substrate (top), followed by SiNWs assembled in between CdSe NWs to form A-B-A-B alternating arrays (bottom) (inset: SEM images showing that both types of NWs after assembly were located at modified molecular pattern locations). This demonstrates that integrated NW assembly can be achieved by the design of complimentary modifications between surfaces of NWs and target substrates. Scale bars in all images: 100 μm.

approach offers substantial promise for building hierarchical structures of NW-based devices necessary for achieving the bottom-up paradigm of nanoscience [3,4].

INTEGRATED NW NANOELECTRONIC SYSTEMS

Developing organized and interconnected high-density arrays of NW building blocks from the bottom-up is central to the efforts directed toward the ultimate realization of assembled nanocomputing systems that represent the revolutionary advances beyond existing semiconductor technology. The rational synthesis of semiconductor NWs with well-defined electronic properties and their hierarchical assembly enable the building of a broad range of functional devices and integrated nanoelectronic systems based on these NW structures.

Crossbar NW memory elements and small-scale 1D memory array

The NW-based crossbar structure represents a powerful and scalable architecture for memory and logic devices in that key device features can be defined during the synthesis of NW building blocks and their subsequent assembly. In a NW crossbar structure, the bit size is defined by the diameters of the orthogonal NWs (readily scaled down to nanometer level) and the electronic characteristics of the functional element are defined by the compositions of the two NWs (e.g., core/shell materials). To illustrate this NW crossbar device concept, we demonstrate the crosspoint hysteretic resistance switches based on core/shell Si NW–metal NW crossbars in which the core of the NW heterostructure acts as one electrode contact, the shell that can be synthetically controlled functions as the information storage medium, and the metal NW serves as the second electrode contact [58].

The basic design of the device structure shown in Fig. 7a consists of a NW heterostructure with crystalline-silicon core (c-Si) and amorphous-silicon (a-Si) shell and a lithographically defined crossed metal NW. The c-Si/a-Si core/shell NWs were synthesized in a gas-phase process developed previously and were configured as crosspoint devices for electrical characterization as follows: (1) the core/shell NWs were assembled on a Si/SiO$_2$ substrate, followed by Ni-metal contacts defined at the NW ends (Ni results in reliable ohmic contacts to Si NWs); (2) an additional lithography step was introduced to define one or more crossed metal NWs.
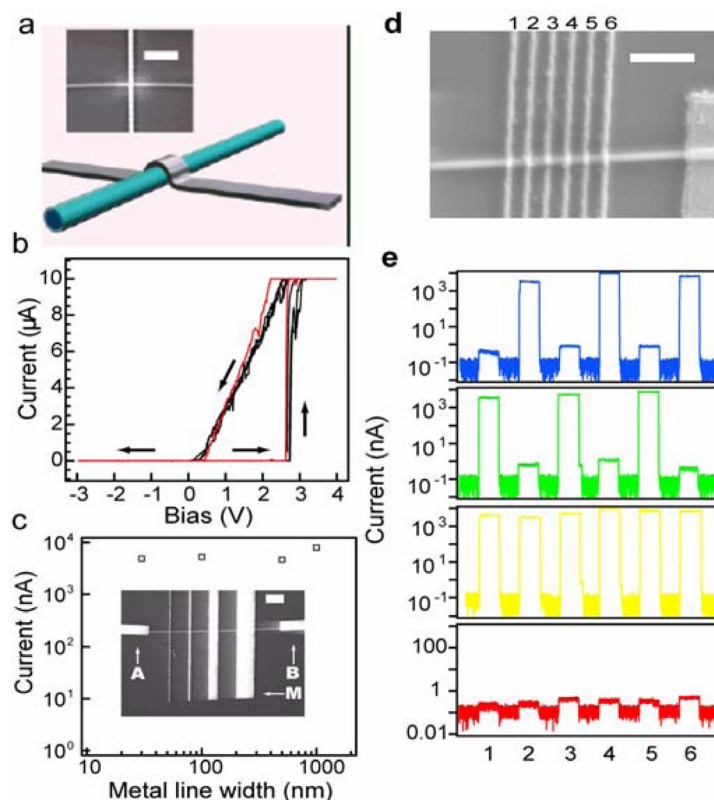

Fig. 7 Crossbar NW memory elements and small-scale 1D memory array. (a) Si/a-Si × metal NW crossbar switch structure; (b) *I–V* sweep curves showing basic switching behavior of crossbar NW element; (c) current read at 1.5 V for devices fabricated with different metal line widths (1 µm and 500, 200, and 30 nm) on a single core/shell NW; (d,e) SEM image of a 1 × 6 array composed of one Si/a-Si NW crossing six Ag lines and corresponding states of crosspoints 1–6 read at 2 V: blue = 010101, green = 101010, yellow = 111111, red = 000000. Scale bar: 500 nm. Adapted from [58].

Room-temperature electrical measurements on single Si/a-Si × Ag NW devices demonstrated the following key features: bistable switching between high (OFF) and low (ON) resistance states with well-defined switching threshold voltages (representative *I–V* data shown in Fig. 7b), ON/OFF ratios > 10^4, and current rectification in the ON state. Furthermore, systematic studies of Si/a-Si × Ag NW devices show that (i) the bit size can be at least as small as 20 × 20 nm (Fig. 7c), (ii) the writing time is <100 ns, (iii) the retention time is >2 weeks, (iv) devices can be switched >10^4 times without degradation in performance.

In addition, the scalability of the Si/a-Si × Ag NW device structure has been investigated in small-scale 1D (1 × 6) arrays. For example, dense 1 × 6 memory arrays were fabricated by crossing one Si/a-

Si NW with 6 electron-beam lithographically defined Ag NWs shown in Fig. 7d, with Ag NW width of 30- and 150-nm spacing. Transport measurements (Fig. 7e) further demonstrated our ability to write/erase the six crosspoint switches to an arbitrary state (e.g., 000000, 111111, 101010, 010101) and then read out the state of six switches without crosstalk between elements during writing, reading, or erasing.

Integrated Si NW-based memory and logic arrays for nanocomputing

To realize the full potential of our Si/a-Si NW × Ag NW crossbar switches, we have made substantial effort to push forward the assembly and integration of highly integrated 2D arrays, which require two sets of high-density parallel NW arrays. First, to prepare dense parallel arrays of Si/a-Si NWs, we have employed the LB method to assemble well-ordered arrays with controlled NW alignment and spacing tunable from several μm down to sub-100 nm [40]. High-density crossbar memory arrays were then successfully completed by fabricating perpendicular high-density metal NWs using high-resolution electron-beam lithography [59]. The merger of top-down lithography and bottom-up assembly that define high-density arrays of metal NWs and Si/a-Si NWs, respectively, offers great promise in efficiently building Si/a-Si × Ag NW crossbar memory arrays.

The point addressability and storage capability of memory array has been tested on a 6 × 6 (36 bit) crossbar NW array confirming uniform memory characteristics achieved with our Si/a-Si × Ag NW-based crossbar system (Fig. 8). Strings of 1s and 0s corresponding to standard ASCII alphanumeric symbols were stored into the array, and subsequently read out. Figure 8c presents the results of such write/read testing. An operational memory is demonstrated by successfully writing and reading out the word "NANO" [e.g., an "N" character (ASCII 78), is represented as the 8-bit number "01001110"]. The bit current read-out from the array is plotted in log scale to show the readily differentiated levels of the "on" and "off" states of all bits within the crossbar circuit, with the 1/0 current ratio in the order of 10^2, an order better than previously reported molecular electronic crossbar circuits [60]. The findings demonstrate that excellent memory characteristics can be achieved with our Si/a-Si × Ag NW-based crossbar system.
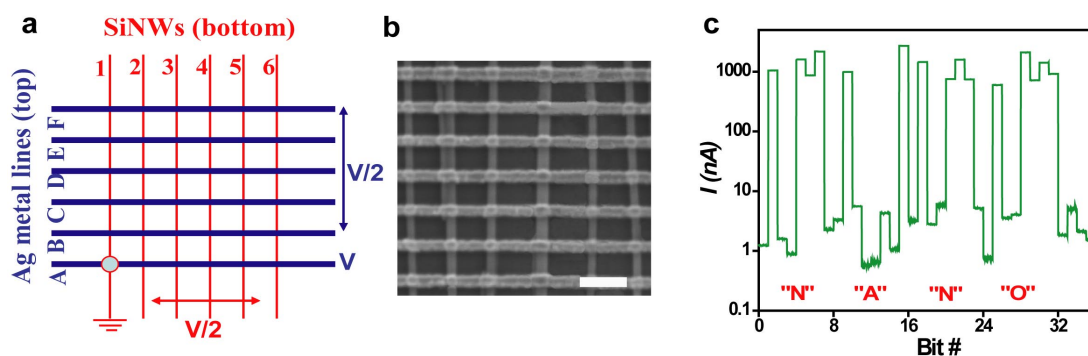

Fig. 8 6 × 6 high-density crossbar NW memory circuit and point addressability demonstration. (a,b) Schematic and SEM image of a 6 × 6 NW crossbar memory structure and Write/Read modes for the memory array; scale bar is 100 nm. (c) The use of 36-bit crossbar memory to store the word "NANO" (ASC II) is demonstrated with read current values plotted on a log scale.

In addition to memory applications, Si/a-Si × Ag NW crossbar structures can be configured to form crossed nanoscale junctions and junction arrays in which the electronic properties and function are controlled in a predictable manner to provide both diode and FET elements in a circuit, which represent two basic device elements in logic gates. To demonstrate the flexibility of these NW device elements, we have used these assembled Si/metal NW crossbar arrays to design and realize both diode- and FET-based logic, including the inverter, AND, NAND, and more complex "product of sums" (POS) logic structures (Fig. 9). For example, an inverter structure was realized by using a 1 Si/a-Si NW × 2 Ag NW crossbar array with one Ag NW working as top-gate metal (gating bottom Si NW through dielectric layer of ZrO_2 selectively deposited by ALD), and the other as contact electrode for the diode switch junction. Representative I–V curves measured on both crossed junctions show that two crosspoints can function as FET (blue curve) and diode switch elements (red curve). Further, by inputting the voltage V_i-biased on top-gate Ag NW and giving a constant V_{sd} (~2 V), the output voltage measured from the diode electrode Ag NW can be tuned from the "high" state when the input voltage is set to low, to the "low" state when the input voltage is set to high (Fig. 9a). A logic AND gate was also assembled from a 2 Si/a-Si NWs × 1 Ag NW array (Fig. 9b), and a logic NAND gate was assembled by using a 3 Si/a-Si NWs × 2 Ag NW array (Fig. 9c). The controlled and predictable assembly of these
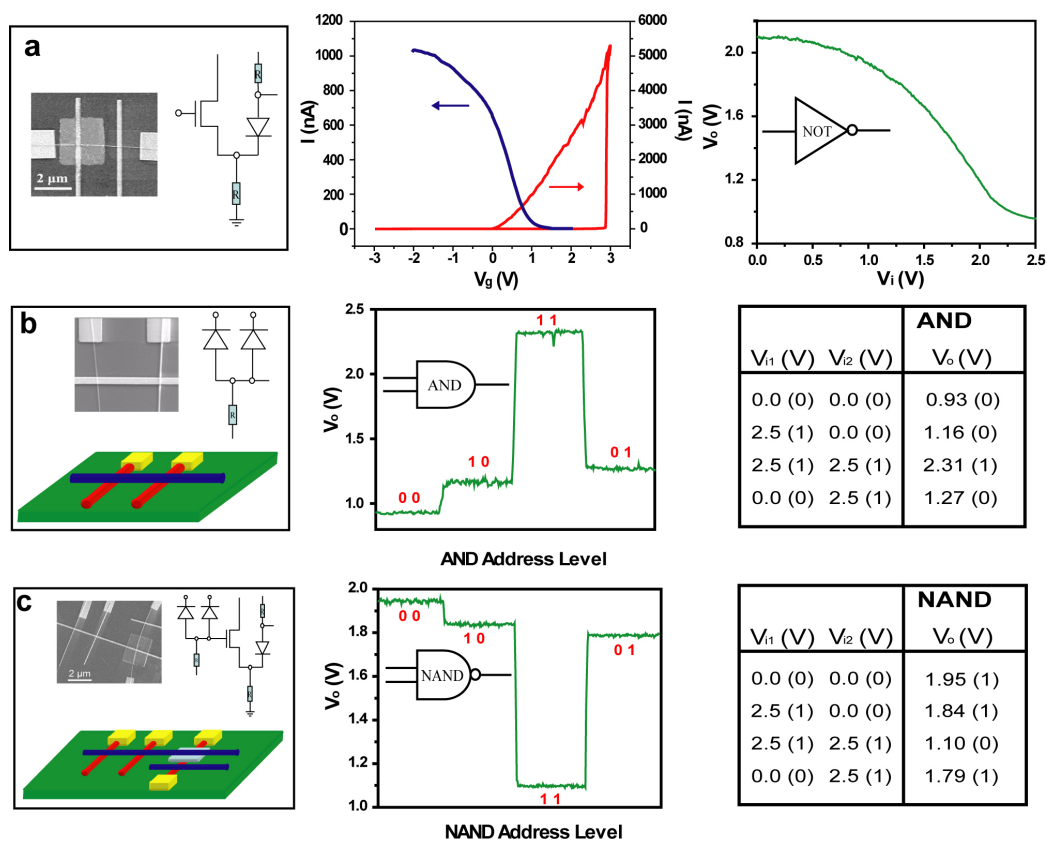

V_{i1} (V)	V_{i2} (V)	AND V_o (V)
0.0 (0)	0.0 (0)	0.93 (0)
2.5 (1)	0.0 (0)	1.16 (0)
2.5 (1)	2.5 (1)	2.31 (1)
0.0 (0)	2.5 (1)	1.27 (0)

V_{i1} (V)	V_{i2} (V)	NAND V_o (V)
0.0 (0)	0.0 (0)	1.95 (1)
2.5 (1)	0.0 (0)	1.84 (1)
2.5 (1)	2.5 (1)	1.10 (0)
0.0 (0)	2.5 (1)	1.79 (1)

Fig. 9 Logic gate structures based on core/shell Si × Ag crossbar NW system. (a) (left) SEM image of assembled inverter structure and symbolic electronic circuit. (middle) I–V curves of both crosspoints showing that both diode switch (red curve) and FET (blue) functions can be achieved using a single Si NW crossing two metal NWs. (right) Output–input relation curve (V_o–V_i). (b,c) (left) Schematic and SEM images for assembled logic AND and NAND gates and their symbolic electronic circuits. (middle) Output voltage vs. four possible logic address level inputs. (right) Experimental truth table for AND and NAND gates.

logic gate structures enables the organization of virtually any logic circuit and represents a substantial advance compared with previous studies of molecular systems [60].

Our NW crossbar approach leads naturally through the bottom-up paradigm to integration at the nanoscale and represents a significant step toward the creation of a more sophisticated nanoelectronic computing system. Although several challenges remain to be solved, including the development of more sophisticated assembly methods for ultradense and more-ordered NW arrays and further improvement in materials synthesis, we are still excited about the potential of NW crossbar-based integrated nanosystems for achieving unparalleled device densities and novel system performance. The development of optimized materials and assembly techniques for fabricating large-scale NW-based integrated circuits and further exploration of novel computing architectures and systems-level implementation represent some directions for future work.

Integrated 3D multifunctional NW electronics

Three-dimensional integrated circuits consisting of multiple layers of active electronic elements offer the potential for more efficient interconnection and information processing, and offer the promise of performance advantages, including higher integration density, faster operation speed, and lower power consumption [61,62]. These significant benefits of 3D integrated circuits have motivated tremendous research in the electronics community and enabled a world of new design possibilities. Although much progress has been made in this field based on conventional Si complementary metal-oxide semiconductor (CMOS) technology, materials- and fabrication-related challenges have still presented major obstacles in achieving truly 3D integrated circuits, and the need for developing a new technology remains critical. Semiconductor NWs and carbon NTs offer an attractive alternative approach to construct novel 3D integrated circuits given the unique capability of assembling these high-performance 1D building blocks with diverse functional properties [3,4].

Our powerful printing method offers the potential for layer-by-layer integration of NW building blocks needed to realize 3D integrated electronics in a new and powerful manner. Through sequential assembly of individual and/or parallel arrays of single-crystalline NWs as multifunctional and multilayer circuits, we have achieved vertically stacked 3D device circuits with up to 10 addressable vertical layers [44]. Specifically, vertically stacked multilayer structures are constructed by multiple iterations of the NW printing and device fabrication steps along with the deposition of an intervening separation layer of insulating film, as schematically shown in Fig. 10a. For example, to explore the assembly and fabrication of multifunctional 3D NW electronics on flexible substrates, we have designed a 3D structure composed of double layers of functional circuits with a bottom layer of inverters and a top layer of floating-gate memory elements (Fig. 10b). An optical image of a typical 3D structure (Fig. 10c) clearly shows the assembled inverter-memory structures on plastic Kapton substrates, using Ge/Si core/shell NWs as the active semiconductor material [63]. Notably, electrical characterization studies demonstrated that the inverters exhibit signal inversion with larger-than-unity gain for frequencies up to at least 50 MHz, the highest reported operation frequency for a circuit made of any channel material on flexible substrates, outperforming a-Si and organic electronics by 2 orders of magnitude [64,65] (Fig. 10d). Further writing and erasing tests on the NW memory devices also showed well-defined and stable ON and OFF states proving excellent memory performance achieved (Fig. 10e).
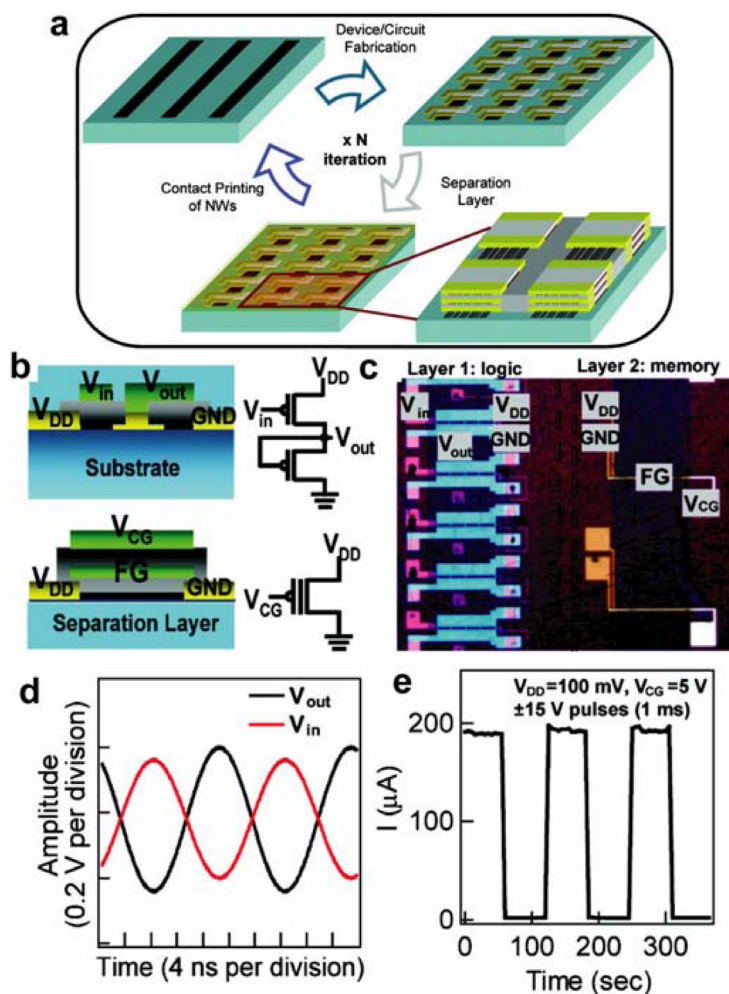
Fig. 10 3D NW integrated circuits. (a) Schematic process showing that 3D NW circuit is fabricated by multiple time iteration of the contact printing, device fabrication, and separation layer deposition steps. (b) Schematics and circuit diagrams of inverter (top) and floating-gate memory (bottom) elements based on assembled NWs. (c) Optical image of inverters (layer 1) and floating-gate memory (layer 2) on Kapton plastic sheets. (d) AC inverter characteristics in layer 1. Gain is larger than unity (V_{in}, red; V_{out}, black) at 50 MHz and V_{DD} of 4 V. (e) Switching characteristics of memory (layer 2) at $V_{CG} = 5$ V with –15 and +15 V pulses (pulsing time, 1 ms). Adapted from [44].

The demonstrated ability to rationally assemble sequential layers of distinct types of NW-based devices coupled with the breadth of NW building blocks could enable the assembly of increasing complex multilayer and multifunctional 3D electronics in the future. Together with a similar approach involving sequential transfer printing of NWs and carbon nanotubes (CNTs) recently reported by Rogers and co-workers [66], these new assembly-based approaches overcome many processing limitations of conventional planar CMOS technology and therefore promise unique opportunities in building the future-generation high-performance 3D integrated circuits based on nanoscale building blocks. More significantly, this sequential layer-by-layer assembly approach has been further exploited to realize the first fully functional 3D CMOS integrated NW circuits based on separate interconnected layers of high-mobility n-type InAs and p-type Ge/Si NW transistors [51]. Notably, we have demonstrated 3D

CMOS inverters with well-controlled switching thresholds and substantial DC gains ~45, as well as vertically interconnected three-stage ring oscillators with oscillation frequencies up to ~110 MHz, which represents the highest-frequency integrated circuit reported for any nanoscale materials. These results truly highlight the flexibility of our bottom-up assembly of distinct nanoscale materials and show substantial promise for future 3D integrated circuits.

FUNCTIONAL NW NANOELECTRONIC–BIOLOGICAL INTERFACES

Frontier research at the interface between nanotechnology and biological sciences offers the promise in producing breakthroughs in both fundamental science and potentially leading to revolutionary technologies [67–70]. These two broad areas of science share a number of natural connections from the similar size scales of building blocks to the common theme of "bottom-up" organization for hierarchical system-level architectures. Among a variety of nanoscale structures that can be potentially interfaced with biological systems, semiconductor NWs represent a well-defined yet versatile nanomaterial system with demonstrated rationally controlled synthesis and electronic properties, and hierarchical assembly and integration [3,4].

In general, the size similarity of NWs and natural nanostructures in biological systems makes NWs a unique choice for creating highly sensitive tools that can probe biological systems [21–23,67,68]. NW electronic devices, configured as high-performance NW-FET-based sensors, have been demonstrated to enable a detection and sensing modality—direct and label-free electrical read-out based on local electrostatic gating of the NW—that is exceptionally attractive for many applications in medicine and the life sciences. To this end, NW-based detection capabilities were first demonstrated in 2001, where pH, calcium ions, and proteins in solution were detected in real time and with high sensitivity [21]. In 2004, reversible binding and unbinding events of single virus particles to antibody-modified NW-FETs was reported [22], showing the first time viruses could be detected at the single-particle level in real time and without the use of fluorescent labels. In 2005 [23] and 2007 [71], antibodies-conjugated NWs were also used to detect their specific antigen proteins at concentrations as low as 3 fM, which represents a sensitivity limit $>10^4$ times below that afforded by state-of-the-art ion planar FETs [72,73]. The NW-enabled nanotechnology truly represents a powerful and general platform for building functional interfaces between nanoelectronic systems and biological systems from proteins, viruses, to cells and tissues, opening up a number of opportunities in the merging field of integrated nanobiotechnology.

Hybrid NW–neuron interfaces

We have investigated the rich interface between nanoelectronic and cellular biological systems, such as neurons, by assembling and studying hybrid structures consisting of NW-FET arrays and patterned neurons [74]. Given the nanoscale contact length (~20 nm) between an axon or dendrite projection and a crossed NW, individual NW devices can serve as highly local and noninvasive probes of neuronal projections, making them very attractive for establishing active interfaces with neurons. To explore the flexibility of our approach to assemble and characterize hybrid NW/neuron devices in which the number and spatial arrangement of NWs interfaced to the axons and dendrites can be varied, we assembled hybrid multi-NW/neurite structures (Fig. 11a) consisting of a central neuron cell body and four peripheral NW elements arranged at the corners of a rectangle with polylysine patterning designed to promote neurite growth across these elements. A representative optical image (Fig. 11a) shows one NW-axon, and two NW-dendrite elements at positions 1, 2, and 3, respectively. Figure 11b shows that stimulation of action potential spikes in the soma yields correlated conductance peaks in the NW/axon (NW1) and NW/dendrite (NW2, NW3) devices, while no signal was observed in a control detector (NW4), showing the absence of cross-talk in the hybrid device array.
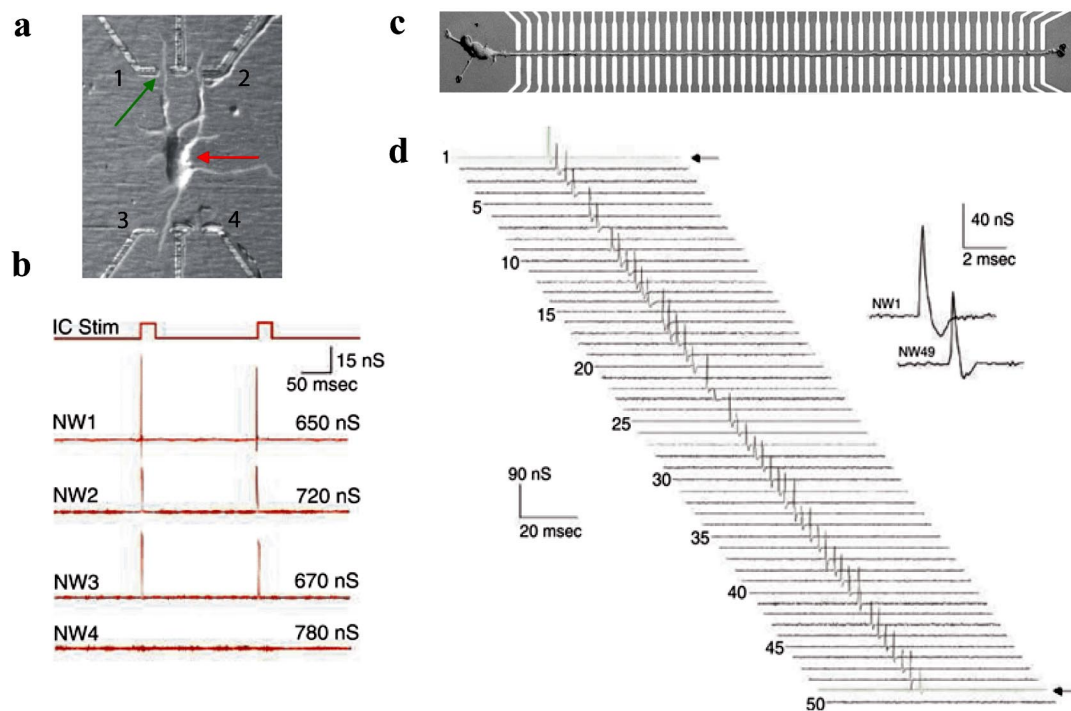
Fig. 11 Multi-NW-neurite structures and highly integrated NW-neuron devices. (a) Optical image of a cortex neuron connected to 3 of the 4 functional NW devices in the array. Two possible stimulation approaches: intracellular stimulation (red arrow in soma) and extracellular NW-based stimulation (green arrow on NW1). (b) Electrical responses measured from NW/neuron junctions after intracellular stimulation. (c) Optical image of aligned axon crossing an array of 50 NW devices with a 10 μm inter-device spacing. (d) Electrical mapping data from 50-device array shown above with yield of functional devices 86 %. Adapted from [74].

Our approach can be readily extended to highly integrated systems, offering a unique advantage over previous works with microfabricated planar FETs and microelectrodes [75,76]. For example, we designed and fabricated a repeating structure that consists of 50 addressable NW elements per neuron, as shown in Fig. 11c, demonstrating an unprecedented level of integration for nanoelectronic–biological systems. An optical image (Fig. 11c) shows that well-aligned neuron growth across high-density NW device arrays was achieved. Moreover, electrical measurements made after neuron growth demonstrated intracellular stimulation of action potentials in the soma yield a mapping of the spike propagation by the 43/50 working devices (86 % device yield) over the 500-μm-long axon (Fig. 11d).

Beyond this demonstration of highly integrated electrical interfacing, we have also used NW/neuron structures to demonstrate novel hybrid electronic devices, including the demonstration of complementary electronics and logic gates [74]. More generally, interfacing multiple NW inputs and outputs to neurons and neural networks enables the stimulation, inhibition, or reversibly blocking of signal propagation along specific pathways while simultaneously mapping signal flow throughout the network. This approach could not only be used to investigate synaptic processing in neural networks and to explore hybrid circuits for information processing [77], but be useful for developing flexible real-time cellular assays, for example, for drug discovery and testing.

Functional NW–heart tissue interfaces

In addition to NW–neuron interface, we used embryonic chicken hearts as a model system to study functional NW–tissue interfaces [78]. Specifically, we fabricated large-scale NW transistor arrays on both planar and flexible and transparent polymeric substrates that can be reproducibly interfaced with spontaneously beating hearts in both 2D and 3D conformations. For example, multiplexed recording from NW-FET arrays yielded signal propagation times across the myocardium with high spatial resolution. More significantly, our transparent and flexible NW-FET chips enable simultaneous optical imaging and electronic recording in 3D configurations that are not readily accessible with traditional planar device chips, yet are critical for producing diverse, functional tissue–device interfaces. To illustrate this capability, a flexible device chip in bent configurations (Fig. 12a) with concave surface facing a beating heart immersed in medium, is readily integrated into an upright microscope and allows for both visual inspection for rough orientation of the device array to the heart and higher-resolution imaging through the transparent substrate while recording from NW-FET devices. The capacity for simultaneous imaging of tissue and devices enables their registration at the level of the entire organ down to that of individual cells (Fig. 12b). Notably, multiplexed device measurements from three representative devices in the array fabricated in a flexible chip on Kapton plastic (Figs. 12c,d) demonstrate excellent S/N peaks correlated with the simultaneous-beating heart with recorded magnitudes of 127 ± 4, 146 ± 4, and 114 ± 4 nS for NW1, NW2, and NW3, respectively. These conductance values correspond to calibrated voltages of 5.3 ± 0.2, 4.6 ± 0.1, and 5.3 ± 0.2 mV. This demonstrates that flexible NW nanoelectronic devices can be interfaced with living cells/tissues to form diverse, functional nanoscale hybrid junctions for spatially resolved, multiplexed, highly sensitive signal recordings. We believe that NW-FET arrays fabricated on increasingly flexible plastic or biopolymer substrates can become unique tools for electrical recordings from other tissue/organs or as powerful implants [79].
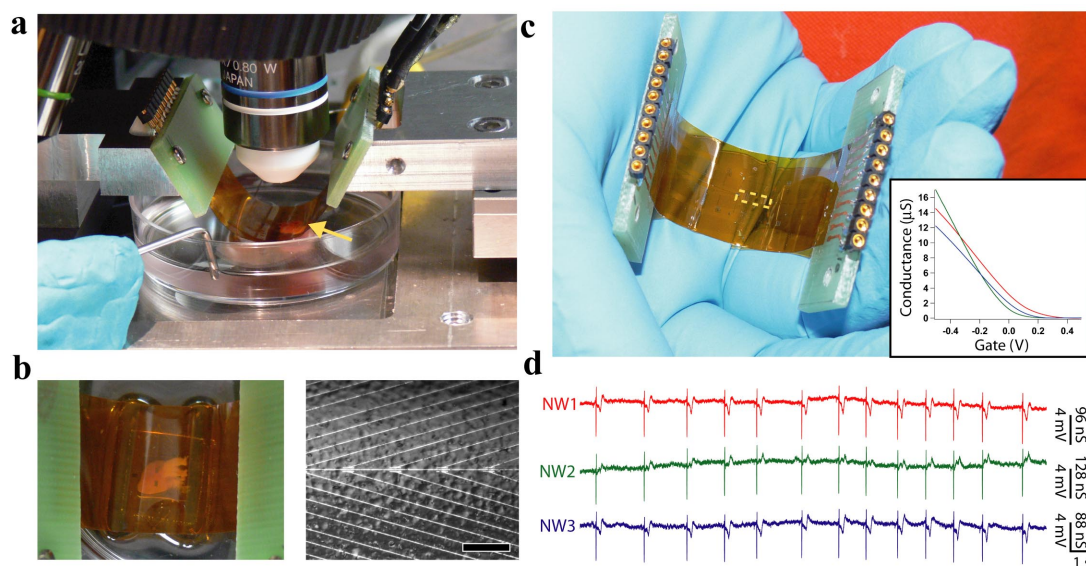

Fig. 12 Multiplexed recording from heart tissue using flexible NW-FET arrays. (a) Photograph of a heart located underneath bent substrate with devices on lower concave face of the substrate. (b) (left) Top-down photograph of same system, enabling registration between heart and devices. (right) Optical image showing features on heart surface vs. position of individual NW devices (scale bar 150 μm). (c) Photograph of complete NW-FET chip fabricated on a flexible Kapton substrate. Inset, water gate G vs. V_g measurements for three typical NW-FET devices. (d) Multiplexed device measurements recorded at $V_g = -0.2$ V. Conductance measurement was calibrated using the corresponding water-gate data shown in c. Adapted from [78].

CONCLUSIONS

This review illustrates a series of key advances in developing methodologies to rationally assemble NW building blocks into designed architectures and further integrating these ordered structures to construct functional NW nanosystems. First, we have developed several unique assembly approaches to organize semiconductor NWs into hierarchically ordered structures, including BBF technique and chemical interactions-directed assembly. Second, we have demonstrated significant progress in building integrated nanoelectronic systems such as high-density memory and logic arrays, and multilayer 3D NW electronics. Third, we have explored functional nanoelectronic–biological interfaces using assembled NW device arrays with examples of highly integrated NW–neuron interface and flexible NW–heart tissue interface. These results clearly demonstrate that NWs are unique and truly powerful building blocks for realizing the promise of the bottom-up paradigm of nanotechnology. We believe that NW-based nanosystems will continue to make revolutionary impacts in many research areas from the life sciences, healthcare, to information technology and energy science in the future.

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